Please amend claims 1,3, 4-6, and 8 by rewriting same to read as follows and cancel claims 2, 7, 14, and 15, without prejudice or disclaimer.

--1. (Twice Amended) An address generator for generating addresses for writing data to a prescribed storage means or reading said data from said prescribed storage means, comprising:

first address data generation means for generating first address data at predetermined address intervals, wherein said first address data generation means includes a counter for counting up to a predetermined number and producing counter outputs and a carry output signal, and a multiplier for generating said first address data at said predetermined address intervals by multiplying each of said counter outputs by a predetermined value;

second address data generating means for generating second address data at said predetermined address intervals in synchronism with said carry output signal from said counter; and

addition means for generating said addresses at said predetermined address intervals by sequentially adding said second address data to said first address data.

--3. (Twice Amended) The address generator according

to Claim 1, wherein said multiplier comprises a shift arithmetic circuit for generating said first address data at said predetermined address intervals by bit shifting predetermined bit positions of said counter outputs of said counter.

--4. (Twice Amended) An interleave unit for rearranging and outputting symbols of a transmit symbol series generated by coding original data comprising:

first address generating means for generating first address data at predetermined address intervals, wherein said first address data generation means includes a counter for counting up to a predetermined number and producing counter outputs and a carry output signal, and a multiplier for generating said first address data at said predetermined address intervals by multiplying each of said counter outputs by a predetermined value;

second address data generating means for generating second address data at said predetermined address intervals in synchronism with said carry output signal from said counter; and

addition means for generating addresses at said predetermined address intervals by sequentially adding said second address data to said first address data; and

control means for rearranging and outputting said symbols of said transmit symbol series at random by sequentially

assigning said addresses at said predetermined intervals to said transmit symbol series.

--5. (Twice Amended) The interleave unit according to claim 4, wherein said control means comprises:

storage means for storing said transmit series symbol series;

writing means for writing said transmit symbol series into said storage means on the basis of said addresses at said predetermined address intervals; and

reading means for reading said transmit symbol series from said storage means in an order different from that of said addresses.

--6. (Twice Amended) The interleave unit according to Claim 4, wherein said control means comprises:

storage means for storing said transmit symbol series;

writing means for writing said symbol series into said storage means in a predetermined write order; and

reading means for reading said transmit symbol series from said storage means on the basis of said addresses at said predetermined intervals.

--8. (Twice Amended) The interleave unit according to

Claim 4, wherein

said multiplier comprises a shift arithmetic circuit for generating said first address data at said predetermined address intervals by bit-shifting predetermined bit positions of said counter outputs of said counter.--